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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/884,595	06/18/2001	Quat T. Vu	42390P10889	3197

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/884,595	VU ET AL.	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) *4,8, 9, 11, 12 and 14-44* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-7, 10, 13 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 09/884595 Attorney's Docket #: 42P10889
Filing Date: 6/18/2001;

Applicant: Vu et al.

Examiner: Alexander Williams

Applicant's Amendment filed 12/29/03 has been acknowledged.

Applicant's drawing has been approved by the Examiner.

Remember: Applicant last elected species I (figures 10-15) filed 6/16/03.

This application contains claims 15-44 drawn to an invention non-elected without traverse.

Note: In claim 8, it was unclear and confusing to what is meant by "wherein said second interconnection layer comprises **at least one dielectric layer abutting at least one of said microelectronic device back surface**, said microelectronic substrate core second surface, and said encapsulant material second surface, and at least one conductive trace disposed on said at least one dielectric layer" as it related to the elected species of figures 10-15. It appears this claim should not be in the elected species, since Applicant provided a new drawing figure 26. This figure would not be grouped with the elected species. Also, claims 4, 11 and 12 relates to a non-elected species.

Therefore, claims 4, 8, 9, 11 and 12 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: detailed above.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 4, 8, 9, 11 and 12 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

The disclosure is objected to because of the following informalities: The related application information should be updated.

Appropriate correction is required.

Claim 2 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, it is confusing to what is meant by "a first interconnection layer disposed proximate said first microelectronic substrate core first surface and said first microelectronic device active surface and further including a second interconnection layer disposed proximate said first microelectronic substrate core second surface and said first microelectronic device back surface, wherein said at least one conductive via electrically connects said first interconnection layer and said second interconnection layer" since claim 1 already claims "a first interconnection layer comprising at least one dielectric layer disposed on said first microelectronic substrate core first surface and at least one conductive trace disposed on said at least one dielectric layer." Are these the same "first interconnection layer" in claims 1 and 2 or are they different?

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 to 3, 5 to 10, 13 and 14, **insofar as claim 2 can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Fillion et al. (U.S. Patent # 5,353,498) in view of Shindo et al. (U.S. Patent # 5,048,179).

In claim 1 and similar claim 10 with the second substrate, Fillion et al. (figures 1 to 8(e)) specifically figure 8(e) show a microelectronic substrate **862**, comprising: a first microelectronic substrate core **834** having a first surface and an opposing second surface, said first microelectronic substrate core having at least one opening defined therein extending from said first microelectronic substrate core first surface to said first microelectronic substrate core second surface; at least one first microelectronic device **832** disposed within said at least one opening, said at least one first microelectronic device having an active surface and a back surface, wherein said first microelectronic device active surface is adjacent said first microelectronic substrate core first surface; a first interconnection layer **840,838** comprising at least one dielectric layer disposed on said first microelectronic substrate core first surface and at least one conductive trace disposed on said at least one dielectric layer; and at least one conductive via **850**

extending from said first microelectronic substrate core first surface to said first microelectronic substrate core second surface. Fillion et al. fail to explicitly show an encapsulation material adhering said first microelectronic substrate core to said at least one first microelectronic device forming a first surface adjacent said microelectronic die active surface and said core first surface and a second surface adjacent said microelectronic die back surface and said core second surface.
13. Fillion et al. (figures 1 to 8e) specifically figure 8e show a microelectronic substrate, comprising: at least one first microelectronic device **832** having an active surface and a back surface; a first interconnection layer **836,838** comprising at least one dielectric layer disposed on said first microelectronic substrate core first surface and at least one conductive trace disposed on said at least one dielectric layer; and at least one conductive via **850** extending from said encapsulation material first surface to said encapsulation material second surface. Fillion et al. fail to explicitly show an encapsulation material forming a first surface adjacent said microelectronic die active surface and a second surface adjacent said microelectronic die back surface.

Shindo et al. is cited for showing an IC chip mounting method. Specifically, Shindo et al. (figures 1a to 28) specifically figure 18 discloses a microelectronic substrate, comprising: a first microelectronic substrate core **42** having a first surface and an opposing second surface, said first microelectronic substrate core having at least one opening defined therein extending from said first microelectronic substrate core first surface to said first microelectronic substrate core second surface; at least one first microelectronic device **50** disposed within said at least one opening, said at least one first microelectronic device having an active surface and a back surface, wherein said first microelectronic device active surface is adjacent said first microelectronic substrate core first surface; a first interconnection layer **60,62** comprising at least one dielectric layer disposed on said first microelectronic substrate core first surface and at least one conductive trace disposed on said at least one dielectric layer; and an encapsulation material **52** adhering said first microelectronic substrate core to said at least one first microelectronic device forming a first surface adjacent said microelectronic die active surface and said core first surface and a second surface adjacent said microelectronic die back surface and said core second surface for the purpose of providing an improved method of mounting an IC on a substrate, wherein the substrate includes a metal plate

which is provided with at least one hole and IC fixed held in position inside of the hole by filling resin material in the gap between the IC chip and the hole.

2. The microelectronic substrate of claim 1, the combination with Fillion et al. has said first interconnection layer **836,838** further disposed proximate said first microelectronic device active surface and further including a second interconnection layer **830,826** disposed proximate said first microelectronic substrate core second surface and said first microelectronic device back surface, wherein said at least one conductive via **850** electrically connects said first interconnection layer and said second interconnection layer.

3. The microelectronic substrate of claim 2, the combination with Fillion et al. further including at least one additional microelectronic device **(other 832)** attached to at least one of said first interconnection layer and said second interconnection layers.

5. The microelectronic substrate of claim 1, the combination with Shindo et al. showing wherein said first interconnection layer **60,62** comprises at least one dielectric layer abutting at least one of said first microelectronic device **(top of 50)** active surface, said first microelectronic substrate core **(top of 42)** first surface, and said encapsulation material **52** first surface, and at least one conductive trace **(850 shown in Fillion et al.)** disposed on said at least one dielectric layer.

6. The microelectronic substrate of claim 5, the combination with Fillion et al. showing at least one conductive trace **844** extends through said at least one dielectric layer to contact at least one electrical contact **15** on said first microelectronic device active surface.

7. The microelectronic substrate of claim 5, the combination with Fillion et al. showing wherein said at least one conductive trace **844** extends through said at least one dielectric layer to contact said at least one conductive via **850**.

8. The microelectronic substrate of claim 2, the combination with Fillion et al. showing wherein said second interconnection layer **830,826** comprises at least one dielectric layer abutting at least one of said microelectronic device back surface, said microelectronic substrate core second surface, and said encapsulant material second surface (Shindo et al. show the encapsulation), and at least one conductive trace **844** disposed on said at least one dielectric layer.

9. The microelectronic substrate of claim 8, the combination with Fillion et al. showing wherein said at least one conductive trace **844** extends through said at least one dielectric layer to contact said at least one conductive via **850**.

14. The microelectronic substrate of claim 13, the combination with Fillion et al. show wherein said first interconnection layer **838,836** disposed is further disposed proximate and said first microelectronic device active surface and further including a second interconnection layer **830,826** disposed proximate said encapsulation material second surface and said first microelectronic device back surface, wherein said at least one conductive via **850** electrically connects said first interconnection layer and said second interconnection layer.

Therefore, it would be obvious to one of ordinary skill in the art at the time of the invention to use Shindo et al.'s encapsulation of the chip in the substrate to modify Fillion et al.'s chip in the substrate for the purpose of providing an improved method of mounting an IC on a substrate, wherein the substrate includes a metal plate which is provided with at least one hole and IC fixed held in position inside of the hole by filling resin material in the gap between the IC chip and the hole.

Response

Applicant's arguments filed 12/29/03 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The insertion of Applicant's additional claimed language, for example, "in claims 1 and 13" cause for further search and consideration to make this action final.

Applicant's amendment necessitated the new grounds of rejection. Accordingly, **THIS ACTION IS MADE FINAL**. See M.P.E.P. § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. § 1.136(a).

A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION

FEE PURSUANT TO 37 C.F.R. § 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

The following references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/782,774,680,700-703, 723,685,686,690-693,696,698,684,796 174/52.1,52.2,52.3,52.4	8/13/03 4/11/04
Other Documentation: foreign patents and literature in 257/782,774,680,700-703, 723,685,686,690-693,696,698,684,796 174/52.1,52.2,52.3,52.4	8/13/03 4/11/04
Electronic data base(s): U.S. Patents EAST	8/13/03 4/11/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
4/11/04

Alexander Williams
Primary Examiner